CTS OPTIMIZATION ON 3D INTEGRATION

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One of the purposes of realizing 3D integration is to reduce the interconnect complexity and delay associated with 2D, which are widely considered as barriers to continued performance gains in future generations. 3D integration has a big impact on all the levels of the flow, starting with the floorplan continuing with the placement, the clock tree synthesis and the routing part. The reduction in wire length enabled a size decrease of the logic gate drivers for these wires, which reduced the distance between logic gates and wire length, causing a "positive effect" that significantly reduce total silicon area.

In this article we have implemented and optimized Clock Tree in a design placed 3D and we have analyzed the results and the impact of reducing wire length on the area, power and timing of the built clock tree. Due to decreasing length of the wires, the number of the buffers and the invertors used to create clock tree is decreasing significantly and optimizing CTS using different strategies leads to a performant clock tree in terms of speed and area. We have chosen to focus on this part of the flow since the Clock Tree Synthesis level holds vital importance in the performance of the entire design. The experimental results show that all the important parameters on CTS like clock-skew, delays and power dissipation are improved compared with existing 2D integration.

Keywords: *3D integration, area reduction, congestion, CTS optimization, skew*

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